

MTD6501A/MTD6501C

3-Phase Brushless Sensorless DC Motor Drivers

1. GENERAL DESCRIPTION

The MTD6501A/MTD6501C are 3-phase full-wave drivers for brushless sensorless DC motors. They feature 180° sinusoidal drive, high torque output, and silent drive. Due to their adaptive features and wide power-supply range capabilities (2 to 14V) they are intended to cover a wide range of motor characteristics, while requiring no external tuning from the user. Speed control can be achieved through either power supply modulation or pulse-width-modulation (using the PWM digital input pin). Due to the compact packaging and minimum bill-of-material (power transistors incorporated, no Hall sensor, no external tuning), they are best suited for low-cost fan applications requiring high efficiency and low acoustic noise, such as CPU cooling fans. Frequency generator output is also included (FG/2 or FG), enabling for precision speed control in closed-loop applications. The MTD6501A/MTD6501C drivers include a lockup protection mode, which turns-off the output current when the motor is under lock condition, and an automatic recovery that enables the fan to run when the lock condition is removed. Motor over-current limitation, short-circuit protection, and thermal-shutdown protection are also included. They are available in a compact thermally-enhanced SOP-8 package.

2. FEATURES

- ◆ Position sensorless BLDC drivers (no Hall sensor required)
- ◆ 180° sinusoidal drive, for high efficiency and low acoustic noise
- ◆ Support 2V to 14V power supplies
- ◆ Speed control through PAM and/or PWM
- ◆ Built-in frequency generator (FG/2 or FG output signal)
- ◆ Built-in lockup protection and automatic recovery circuit (external capacitor not necessary)
- ◆ Built-in over current limitation and short circuit protection
- ◆ Built-in thermal shutdown protection
- ◆ Thermally enhanced SOP-8 package
- ◆ No external tuning required

3. BLOCK DIAGRAM

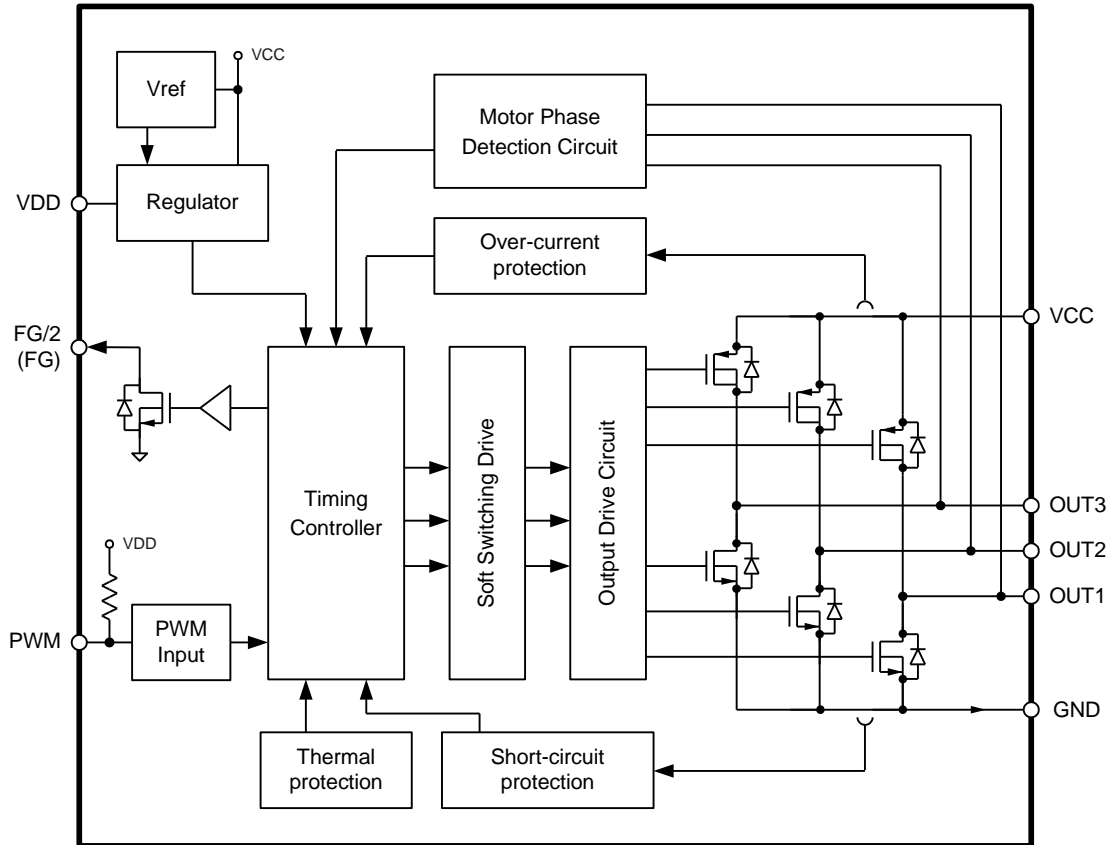


Figure 1: MTD6501A/MTD6501C block diagram

4. SIGNAL DESCRIPTIONS

Table 1: Signal descriptions

SYMBOL	TYPE ⁽¹⁾	PIN #	DESCRIPTION
VCC	P	7	Positive voltage supply for motor driver.
GND	P	5	Negative voltage supply (ground).
OUT1	O	3	Single phase coil output pin.
OUT2	O	4	Single phase coil output pin.
OUT3	O	6	Single phase coil output pin.
PWM	I	8	PWM input signal for speed control.
FG/2 (FG)	O	1	Motor speed indication output (MTD6501A: FG/2, MTD6501C: FG).
VDD	P	2	Internal regulator output (for decoupling only).

Note: (1) I: Input, O: Output, P: Power

4.1. Pin assignments

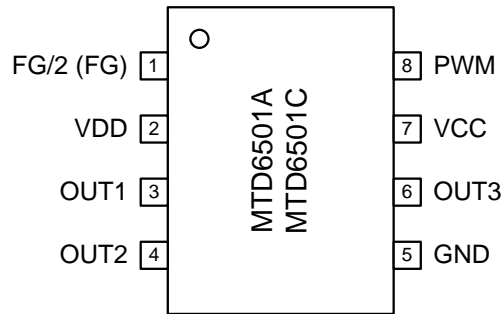


Figure 2: MTD6501A/MTD6501C SOP-8 EP pin assignments

5. FUNCTIONAL DESCRIPTION

The MTD6501A/MTD6501C generate a full-wave signal to drive a 3-phase sensorless BLDC motor. High efficiency and low-power consumption are achieved due to DMOS transistors and synchronous rectification drive type. The current carrying order of the outputs is as follows: OUT1 -> OUT2 -> OUT3.

5.1. Speed control

The rotational speed of the motor can be controlled either through the PWM digital input signal or by acting directly on the power supply (VCC). When the PWM signal is "High" (or left open) the motor rotates at full speed. When the PWM signal is "Low" the motor is stopped (and the IC outputs are set to high-impedance). By changing the PWM duty cycle, the speed can be adjusted. Notice that the PWM frequency has no special meaning for the motor speed and is asynchronous with the activation of the output transistors. Thus the user has maximum freedom to choose the PWM system frequency within a wide range (from 20Hz to 100kHz), while the output transistor activation always occurs at a fixed rate (20kHz, typ.) which is outside of the range of audible frequencies.

5.2. Frequency Generator Function

The Frequency Generator output (FG/2 or FG) is a "Hall-sensor equivalent" digital output, giving information to an external controller about the speed and phase of the motor. The FG/2 (FG) pin is an open collector output, connecting to a logical voltage level through an external pull-up resistor. When a lock (or out-of-sync) situation is detected by the driver, this output is set to high-impedance until the motor is restarted. Leave the pin open when not used.

Table 2: Frequency generator (FG) output options

PRODUCT NAME	FG OPTION
MTD6501A	FG/2
MTD6501C	FG

5.3. Lockup Protection and Automatic Restart

If the motor is stopped (blocked) or if it loses synchronization with the driver, a lock-up protection circuit detects this situation and disables the driver (by setting its outputs to high-impedance) in order to prevent the motor coil from burnout. After a "waiting time" (T_{WAIT}), the lock-up protection is released and normal operation resumes for a given time (T_{RUN}). In case of the motor is still blocked, a new period of waiting time is started. T_{WAIT} and T_{RUN} timings are fixed internally, so that no external capacitor is needed.

5.4. Over current protection and short-circuit detection

The motor peak current is limited by the driver to a fixed value (defined internally), thus limiting the maximum power dissipation in the coils. The detection of a short-circuit situation immediately sets the driver outputs to high impedance, in order to avoid permanent damage to the IC.

5.5. Thermal Shutdown

The MTD6501A/MTD6501C have a thermal protection function which detects when the die temperature exceeds $T_J=170^{\circ}\text{C}$. When this temperature is reached, the circuit enters the thermal shutdown mode and the outputs OUT1, OUT2 and OUT3 are disabled (high impedance), avoiding IC destruction and allowing the circuit to cool down. Once the junction temperature (T_J) has dropped below 145°C , the normal operation resumes (thermal detection circuit has 25°C hysteresis function).

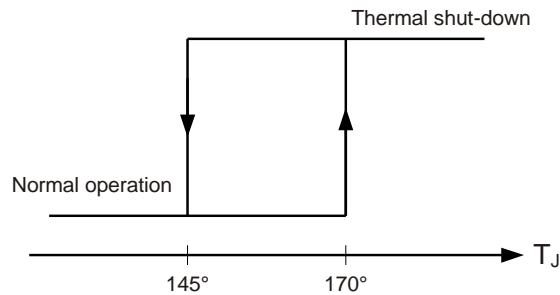


Figure 3: Thermal protection hysteresis

5.6. Internal voltage regulator

VDD voltage is generated internally and is used to supply internal logical blocks. The VDD pin is used to connect an external decoupling capacitor ($1\mu\text{F}$ or higher). Notice that this pin is for IC internal use and is not designed to supply DC current to external blocks.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute maximum ratings

Table 3: Absolute maximum ratings

PARAMETER	SYMBOL	RATINGS	UNIT
Power supply voltage	VCCmax	-0.7 to 15.3	V
Maximum OUT1, 2, 3 output voltage	VOUTmax	-0.7 to VCC+0.7	V
Maximum OUT1, 2, 3 output current (continuous, 100% duty-cycle)	IOUTmax	0.8	A
FG maximum output voltage	VFGmax	-0.7 to 15.3	V
FG maximum output current	IFGmax	5.0	mA
VDD maximum voltage	VDDmax	-0.7 to +4.0	V
PWM maximum voltage	VPWMmax	-0.7 to +4.0	V
Allowable power dissipation ⁽¹⁾	Pdmax	1	W
Operating temperature	Topr	-10 to +85	°C
Max junction temperature	Tjmax	150	°C
Storage temperature	Tstg	-55 to +150	°C

- Note:**
- (1) Reference PCB, according to JEDEC standard EIA/JESD 51-9.
 - (2) De-rating applies for ambient temperatures outside the specified operating range (ref. Figure 4).

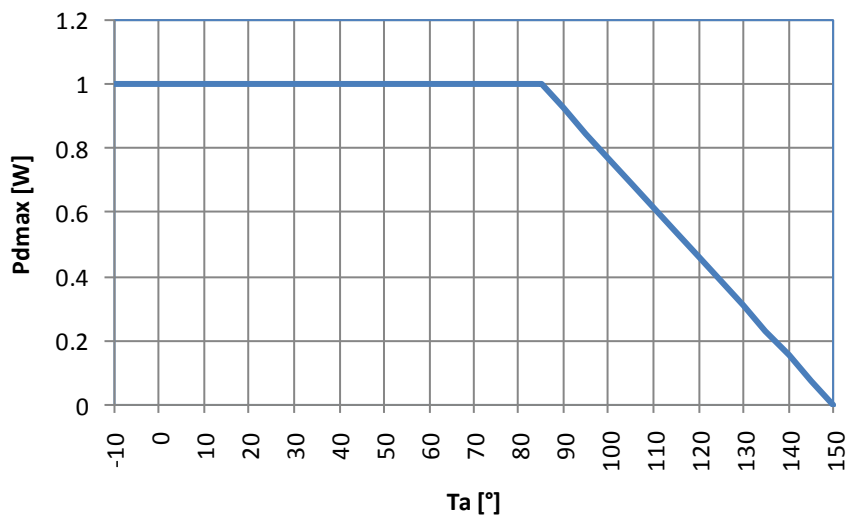


Figure 4: Allowable power dissipation (Pdmax) as a function of ambient temperature (Ta).

6.2. Recommended operating conditions

Table 4: Recommended operating conditions

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply voltage	VCC		2		14	V

6.3. Electrical characteristics

Table 5: Electrical characteristics (Ta=25°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply current	IVCC	Rotation mode		TBD	TBD	mA
		Lock-protection mode		TBD	TBD	mA
OUTx high resistance	Ron(H)	I _{OUT} = 0.5A, VCC = 3.3V to 14V		0.75	1	Ω
OUTx low resistance	Ron(L)	I _{OUT} = -0.5A, VCC = 3.3V to 14V		0.75	1	Ω
OUTx total resistance	Ron(H+L)	I _{OUT} = 0.5A, VCC = 3.3V to 14V		1.5	2	Ω
VDD output voltage	VDD	VCC = 3.3V to 14V		3		V
		VCC < 3.3V		VCC-0.2		V
PWM input frequency	f _{PWM}		0.02		100	kHz
PWM input H level	VPWMH		0.8*VDD		3.6	V
PWM input L level	VPWML		0		0.2*VDD	V
PWM internal pull-up current	IPWML	PWM = GND, VCC = 3.3V to 14V	17	34		μA
		PWM = GND, VCC < 3.3V	8	17		μA
FG output pin low level voltage	VOL _{FG}	IFG = -1mA			0.25	V
FG output pin leakage current	I _{IHFG}	VFG = 14V			10	μA
Lock protection operating time	T _{Run}		TBD	0.5	TBD	s
Lock protection waiting time	T _{WAIT}		4.5	5	5.5	s
Thermal shutdown	ThSD			170		°C
Thermal shutdown hysteresis	ΔThSD			25		°C

7. APPLICATION NOTES

Below is an example of application of the fan motor driver.

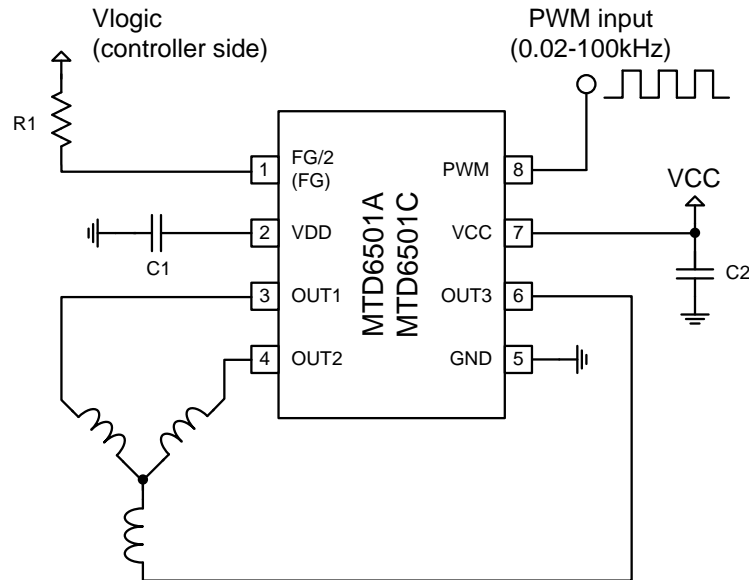
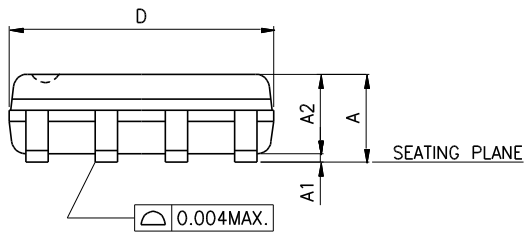
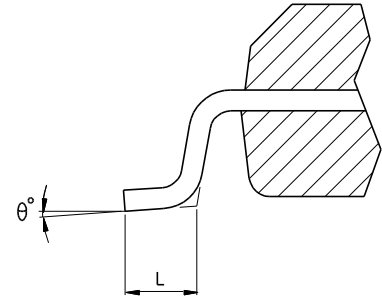
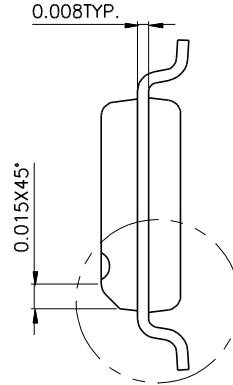
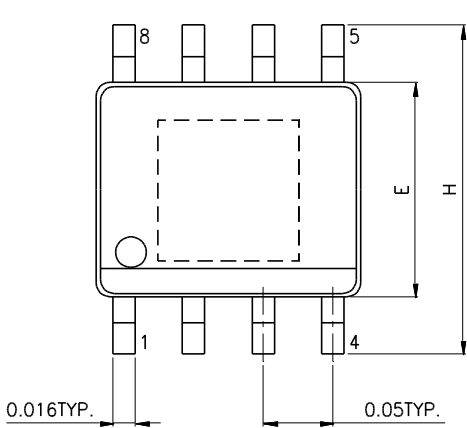


Figure 5: Application example of MTD6501A/MTD6501C

Table 6: Recommended external components for typical application

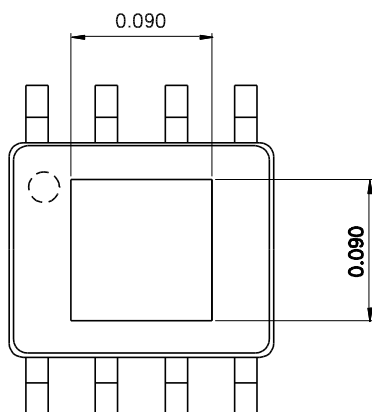
ELEMENT	TYPE/VALUE	COMMENT
C1	$\geq 1\mu\text{F}$	Connect as close as possible to IC input pins
C2	$\geq 1\mu\text{F}$	Connect as close as possible to IC input pins
R1	$\geq 10\text{k}\Omega$	Connect to Vlogic on controller side

8. PACKAGE OUTLINE



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.000	0.006
A2	—	0.059
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH



NOTES:

1. JEDEC OUTLINE : N/A
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

SYMBOL	DESCRIPTION	Conditions	VALUE	UNIT
Theta_JA	Thermal resistance Junction-to-Ambient	Reference PCB, according to JEDEC standard EIA/JESD 51-9	65	°C/W
Theta_JC	Thermal resistance Junction-to-Casing		TBD	°C/W

9. REVISION HISTORY

DATE	REVISION #	DESCRIPTION
August 08, 2007	0.01	Tentative datasheets initial release
May 09, 2008	0.02	Mayor review
June 13, 2008	0.03	Internal review (minor corrections)
June 19, 2008	0.04	Adapted for MTD6501A and MTD6501C products
June 27, 2008	0.05	Corrected IPWML values
July 04, 2008	0.06	Formatting
September 16, 2008	0.07	Temperature range revised
September 19, 2008	0.08	Contact information updated
October 10, 2008	0.09	Changed default value for FG output (high impedance when motor stopped)
December 24, 2008	1.0	Preliminary datasheet

10. DISCLAIMER

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