ADVANCED SILICON

Data Sheet

ASTLC5202A

RGB 480-channels TFT-LCD Source Driver

1. GENERAL DESCRIPTION

The ASTLC5202A is a source driver for AV type color TFT LCDs, i.e. with analog R, G, B video interfaces. The video signals are sampled and held serially, then sent out synchronously through parallel output channels. A clock selection function is provided in order to simplify circuit applications.

This chip provides a 480/402 channels-select function as well as bi-directional shift control for easier circuit layout and cascade function for dot-expansion.

For superior display qualities the output voltages have a dynamic range close to full scale. And for COG applications, special pin locations and dummy pads are supported. That can enhance reliability and performance.

2. FEATURES

- Source driver for AV type TFT LCD panels
- 480(RGBx160) or 402(RGBx134) output channels
- Digital supply: 2.5V - 5.5V
- LCD supply: 3V - 5.5V
- Dynamic range of outputs: 0.2V - 4.8V
- Voltage deviation of outputs: ± 20mV
- Dual sample and hold circuit
- Three or one clock signal alternative
- Cascade function for dot-expansion
- Right and left shift capability
- Switchable R, G, B signals for different types of color filters
- Output enable signal edge selectable
- Bare chip with gold bumps for COG applications

3. BLOCK DIAGRAM

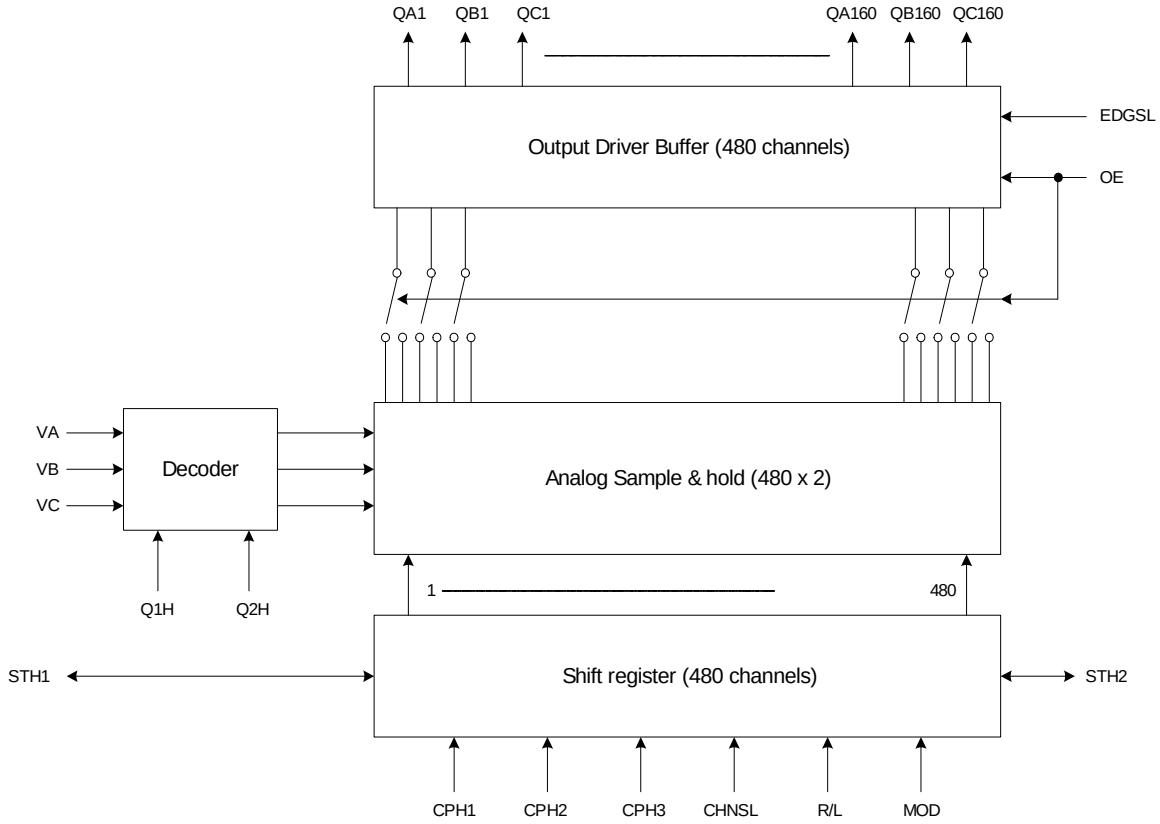

Figure 1: ASTLC5202A block diagram

4. SIGNAL DESCRIPTIONS

Table 1: Pin descriptions

SYMBOL	TYPE	DESCRIPTION
CPH1	I	Clock signal for latching video inputs. R/L = "H": The input data Vx (x=A,B,C depending on Q1H&Q2H) is sampled on the rising edge of CPH1 and hold into embedded buffers sequentially from QA1 to QA160. R/L = "L": The input data Vx (x=A,B,C depending on Q1H&Q2H) is sampled on the rising edge of CPH1 and hold into embedded buffers sequentially from QC160 to QC1.
CPH2	I	Clock signal for latching video inputs. The input data Vx (x=A,B,C depending on Q1H&Q2H) is sampled on the rising edge of CPH2 and hold into embedded buffers. R/L = "H": the data is hold sequentially from QB1 to QB160. R/L = "L": the data is hold sequentially from QB160 to QB1. *Remark: When MOD= "H", CPH2 and CPH3 must be shorted to VDD or VSS.

<table>
<tr><th>SYMBOL</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>CPH3</td><td>I</td><td>Clock signal for latching video inputs.
R/L = ”H”: The input data Vx (x=A,B,C depending on Q1H&Q2H) is sampled on the rising edge of CPH3 and hold into embedded buffers sequentially from QC 1 to QC160.
R/L = ”L”: The input data Vx (x=A,B,C depending on Q1H&Q2H) is sampled on the rising edge of CPH3 and hold into embedded buffers sequentially from QA160 to QA1.
*Remark: When MOD= “H”, CPH2 and CPH3 must be shorted to VDD or VSS.</td></tr>
<tr><td>R/L</td><td>I</td><td>Selects left or right shift; please refer to the description of STH1, STH2.
R/L = "H": STH1 → QX1 → QX2 → QX3 → QX159 → QX160 → STH2
R/L = "L": STH1 ← QX1 ← QX2 ← QX3 ← QX159 ← QX160 ← STH2
<table><tr><th>R/L</th><th>STH1</th><th>STH2</th><th>SHIFT</th></tr><tr><td>H</td><td>IN</td><td>OUT</td><td>RIGHT</td></tr><tr><td>L</td><td>OUT</td><td>IN</td><td>LEFT</td></tr></table>H: High level (VDD) In: Input
L: Low level (VSS) Out: Output</td></tr>
<tr><td>CHNSL</td><td>I
(pull-down)</td><td>Selects the number of output channels.
The timing of the outgoing STHx signal depends on the state of CHNSL.
<table><tr><th>CHNSL</th><th>Output Channel No.</th><th>Note</th></tr><tr><td>H</td><td>402 channels; Qx68~Qx93 are unavailable</td><td></td></tr><tr><td>L</td><td>480</td><td>Default</td></tr></table></td></tr>
<tr><td>STH1
SHT2</td><td>I/O</td><td>A start pulse is applied to STHx when video data is available for sampling.
During a right shift (R/L = "H") the start pulse must be applied to STH1. The data is sampled and hold serially from QA1 to QC160. After the data is completely sampled, i.e. after 160/134 clock cycles, a pulse is shifted out from STH2. This signal can be used to trigger the next chip, and hence to cascade two or more devices to realize a dot-expansion function.
During a left shift (R/L = "L") the start pulse must be applied to STH2 and the end pulse appears in STH1 after 160/134 clocks. The data is serially applied from QC160 to QA1.</td></tr>
<tr><td>OE</td><td>I</td><td>Enables the outputs QA1 to QC160. The dual sample & hold circuit is switched on the rising or the falling edge of OE (depending on EDGSL). During the OE impulse (high or low state depending of EDGSL), the outputs QA1 to QC160 are in Hi-Z state.</td></tr>
<tr><td>EDGSL</td><td>I
(pull-down)</td><td>Selects the active edge of the output enable signal (OE).
EDGSL = “H”: the output enable signal (OE) is active on the falling edge.
EDGSL = “L”: the output enable signal (OE) is active on the rising edge.</td></tr>
<tr><td>MOD</td><td>I
(pull-down)</td><td>Selects which clock signal samples the R, G, B video inputs.
MOD = “L”: The R, G, B signals are sampled sequentially on the rising edge of CPH1, CPH2 and CPH3.
MOD= “H”: The R, G, B signals are sampled simultaneously on the rising edge of CPH1.</td></tr>
<tr><td>VA
VB
VC</td><td>I</td><td>Analog R, G, B video data input</td></tr>
<tr><td>Q1H
Q2H</td><td>I
(pull-down)</td><td>Controls the relationship between the signals VA, VB, VC and the outputs, QAn, QBn, QCn, as shown below. This switchable function is useful to match different types of color filters.
<table><tr><th rowspan="2">Q1H</th><th rowspan="2">Q2H</th><th colspan="3">Output (n=1 to 160)</th></tr><tr><th>QAn</th><th>QBn</th><th>QCn</th></tr><tr><td>L</td><td>L</td><td>VA</td><td>VB</td><td>VC</td></tr><tr><td>L</td><td>H</td><td>VC</td><td>VA</td><td>VB</td></tr><tr><td>H</td><td>X</td><td>VB</td><td>VC</td><td>VA</td></tr></table>X: Regardless</td></tr>
<tr><td>QA1 - QA160
QB1 - QB160
QC1 - QC160</td><td>O</td><td>Output signals to drive LCD panel</td></tr>
</table>

SYMBOL	TYPE	DESCRIPTION
AVDD	P	Analog power supply
VDD	P	Digital power supply
AVSS	P	Analog ground
VSS	P	Digital ground
ALIGN_MARK1,2	-	For assembly alignment
PASS	-	Internally linked together
TP1-TP4	T	Test pins. TP1 and TP2 are shorted; TP3 and TP4 are shorted.
Dummy Pad	-	For COG assembly

Type: I: Input pin, O: Output pin, I/O: Input/Output pin, P: Power pin, T: Test pin, -: For assembly

4.1. Pin assignments

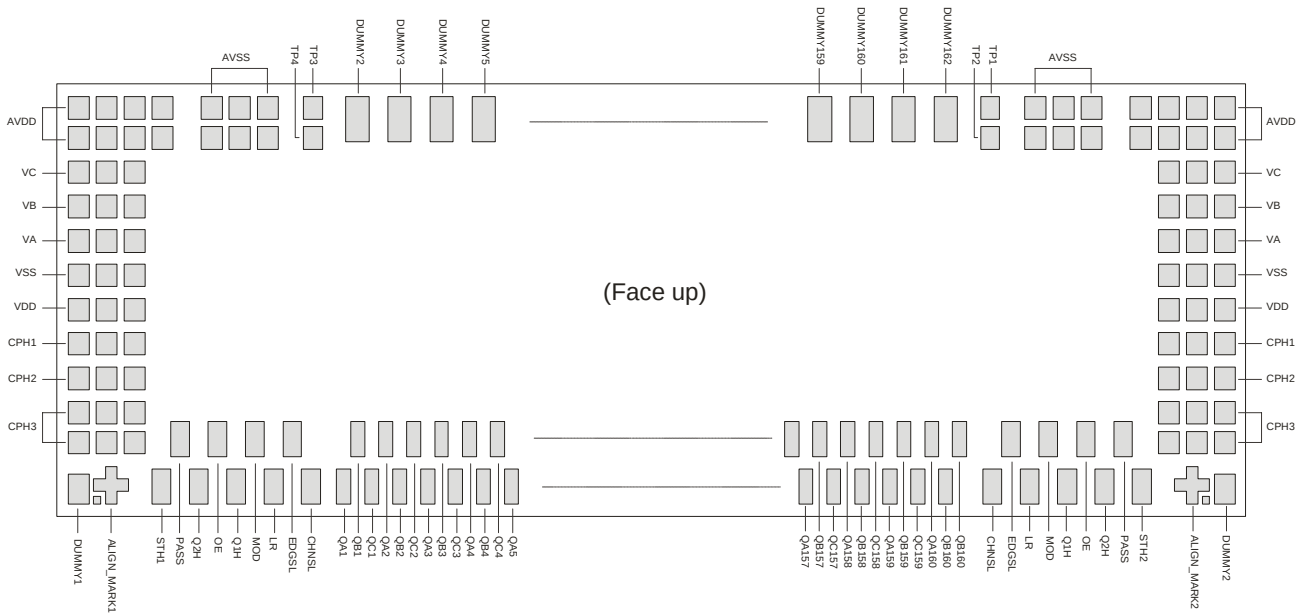

Figure 2: ASTLC5202A pin assignments

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute maximum ratings

Table 2: Absolute maximum ratings

PARAMETER	SYMBOL	RATINGS
DC Supply Voltage	VDD, AVDD	-0.3V to +7.0V
Video Input Voltage	VA, VB, VC	-0.2V to AVDD +0.2V
Digital Input Voltage	V_I	-0.3V to VDD+0.3V
Operating Ambient Temperature	T_A	-20℃ to 75℃
Storage Temperature	T_{STR}	-55℃ to+125℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics

5.2. DC characteristics

Table 3: DC characteristics (VDD = 2.5V - 5.5V, AVDD = 3.0V - 5.5V, T_A = 25°C)

PARAMETER	SYMBOL	LIMIT			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
Analog Supply	AVDD	3.0	-	5.5	V	
Digital Supply	VDD	2.5	-	5.5	V	
Digital Input Low Level	V_{IL}	0	-	0.3xVDD	V	CPH1-CPH3, OE, R/L, STH1, STH2, Q1H, Q2H, MOD, CHNSL, EDGSL
Digital Input High Level	V_{IH}	0.7xVDD	-	VDD	V	CPH1-CPH3, OE, R/L, STH1, STH2, Q1H, Q2H,
Digital Input Leakage Current	I_{IN}	-	-	±1.0	μA	CPH1-CPH3, OE, STH1, STH2, R/L, MOD
Digital Output High Level	V_{OH}	VDD-0.4	-	VDD	V	IOH = -400μA ; STH1, STH2
Digital Output Low Level	V_{OL}	0	-	0.4	V	IOL = 400μA; STH1, STH2,
Video Input Voltage Range	V_{VDO}	-	-	AVDD-0.4	V	VA, VB, VC
Output Dynamic Range	V_{DR}	AVDD-0.4	-	-	V	QA1 to QC160, AVDD= 5.0V
Output Voltage Deviation	V_{VD}	-	±20	-	mV	QA1 to QC160 in V_{DR} range
Output DC offset	V_{OS}	-	-	±20	mV	VA/VB/VC to QAx ~ QCx
Output Current (high output)	I_{OH}		40	-	μA	QA1 to QC160, V_O = 4.8V v.s 4.0V
Output Current (low output)	I_{OL}		40	-	μA	QA1 to QC160, V_O = 0.2V v.s 1.0V
Output Leakage Current	I_O	-	-	±1.0	μA	QA1 to QC160 at high impedance
Pull-down Resistor	R_I		100K	200K	Ω	EDGSL, Q1H, Q2H, MOD, CHNSL
Supply Current (analog)	I_{AVDD}	-	1.2	2.0	mA	F_{CPH} = 5.0MHz, F_{OE} = 15.7KHz, no load
Operating Current (digital)	I_{DD}	-	0.6	1.5	mA	F_{CPH} = 5.0MHz, F_{OE} = 15.7KHz, no load
Stand-by Current (digital)	I_{ST}	-	-	50	μA	Clock & all functions are stopped

5.3. AC characteristics

Table 4: AC characteristics (VCC = 2.5V - 5.5V, AVDD = 5.0V, T_A = 25°C)

PARAMETER	SYMBOL	LIMIT			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
Clock cycle time	T_{CPH}	100	-	2,000	ns	CPHn
CPHn pulse duty	T_{CWH}	40	-	60	%	CPHn
CPHn phase delay	T_{C12} T_{C23} T_{C31}	20	-	T_{CPH}/2	ns	CPH1-CPH2 CPH2-CPH3 CPH3-CPH1
Set-up time of analog signals	T_{ASU}	60	-	-	ns	VA, VB, VC-CPHn
Hold time of analog signals	T_{AHD}	40	-	-	ns	CPHn-VA, VB, VC
STHn set-up time	T_{SU}	20	-	-	ns	STHn-CPHn
STHn hold time	T_{HD}	10	-	-	ns	CPHn-STHn
Propagation delay of STHn	T_{PHL}	10	35	50	ns	CL = 25pF
Sample and hold disable time	T_{DIS}	1	-	-	T_{CPH}	OE-STHn
OE pulse width	T_{WOE}	1	-	-	T_{CPH}	
Settling time	T_{ST}	-	12	20	us	96% final value or precision ≦ 30mV, CL = 60pF

5.4. Timing Diagrams

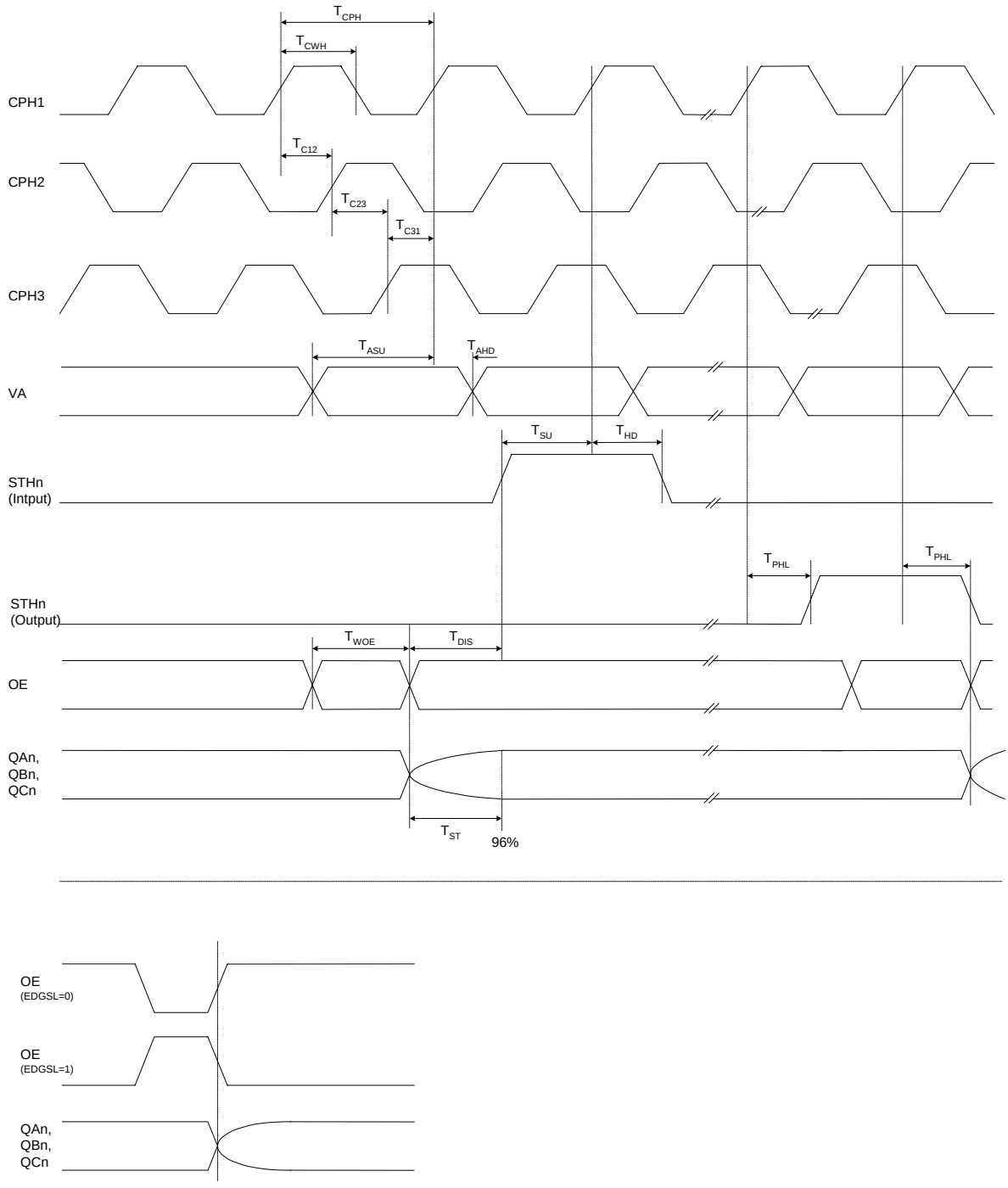

Figure 3: Main waveforms

Remark: The sample-and-hold circuits are switched and the outputs are started with new data at the rising edge of OE.

5.5. Main operating modes

5.5.1. CHNSL = “L”, Q1H = Q2H= “L”, MOD = “L”, R/L = “H”:

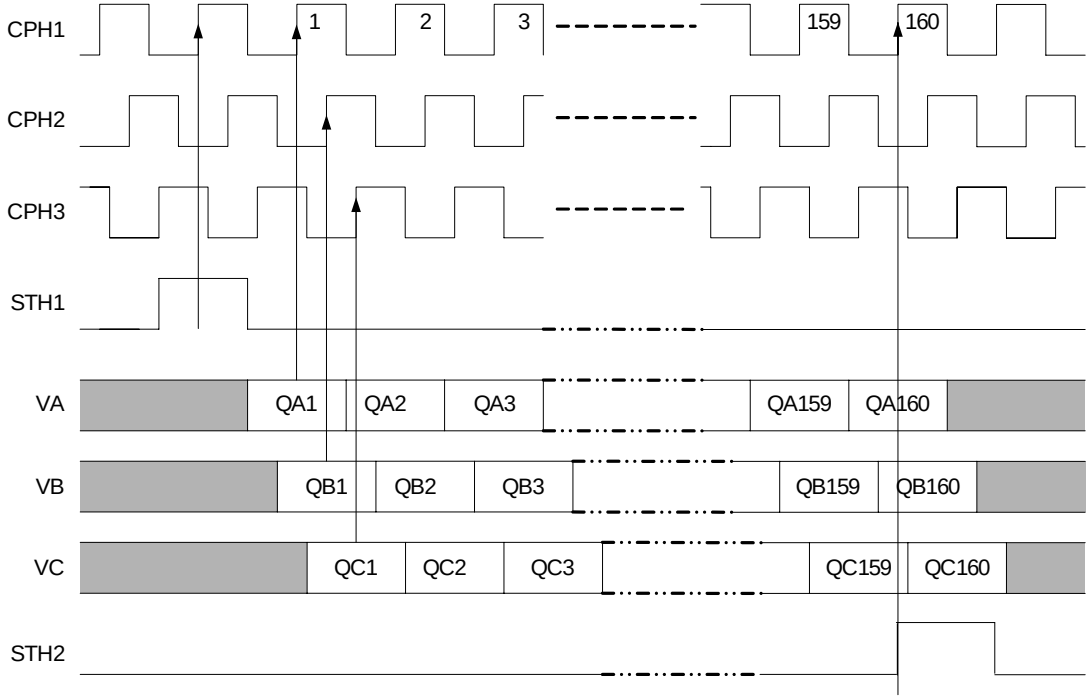

Figure 4: Sequential data acquisition, right shift

5.5.2. CHNSL = “L”, Q1H = Q2H= “L”, MOD = “L”, R/L = “L”:

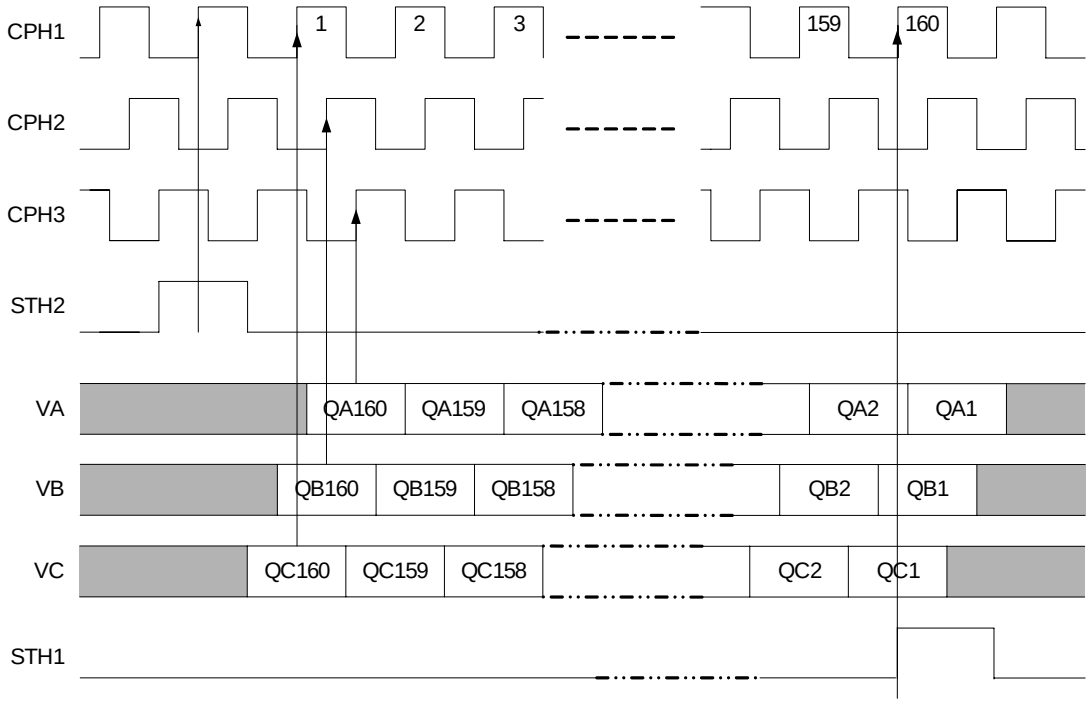

Figure 5: Sequential data acquisition, left shift

5.5.3. CHNSL = “L”, Q1H = Q2H = “L”, MOD = “H”, R/L = “H”:

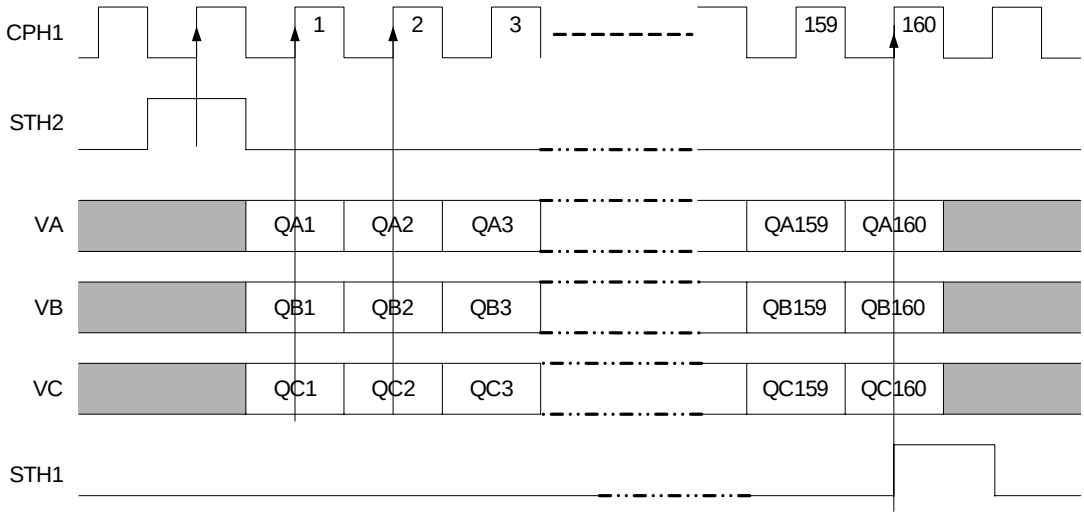

Figure 6: Simultaneous data acquisition, right shift

5.5.4. CHNSL = “L”, Q1H = Q2H = “L”, MOD = “H”, R/L = “L”:

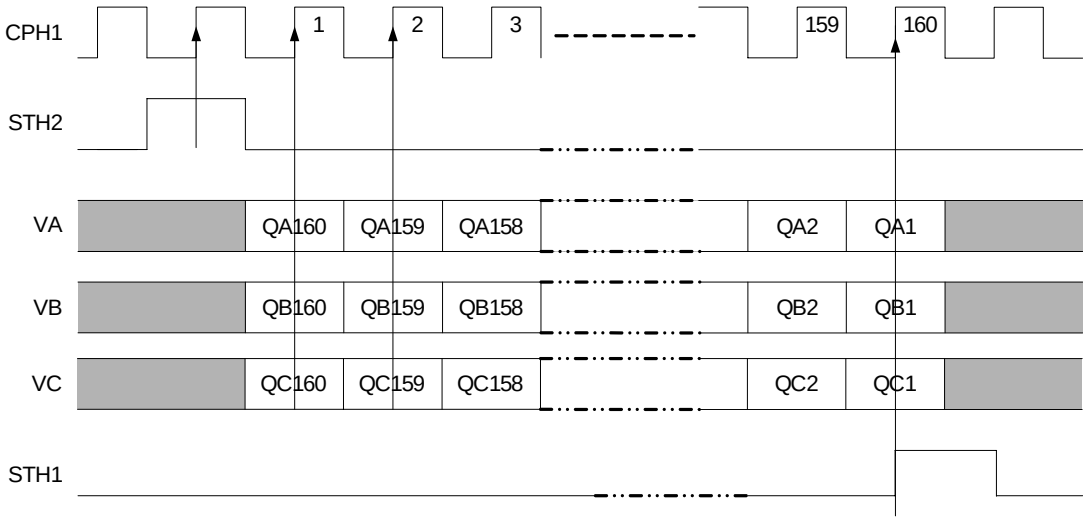

Figure 7: Simultaneous data acquisition, left shift

6. PACKAGE OUTLINE

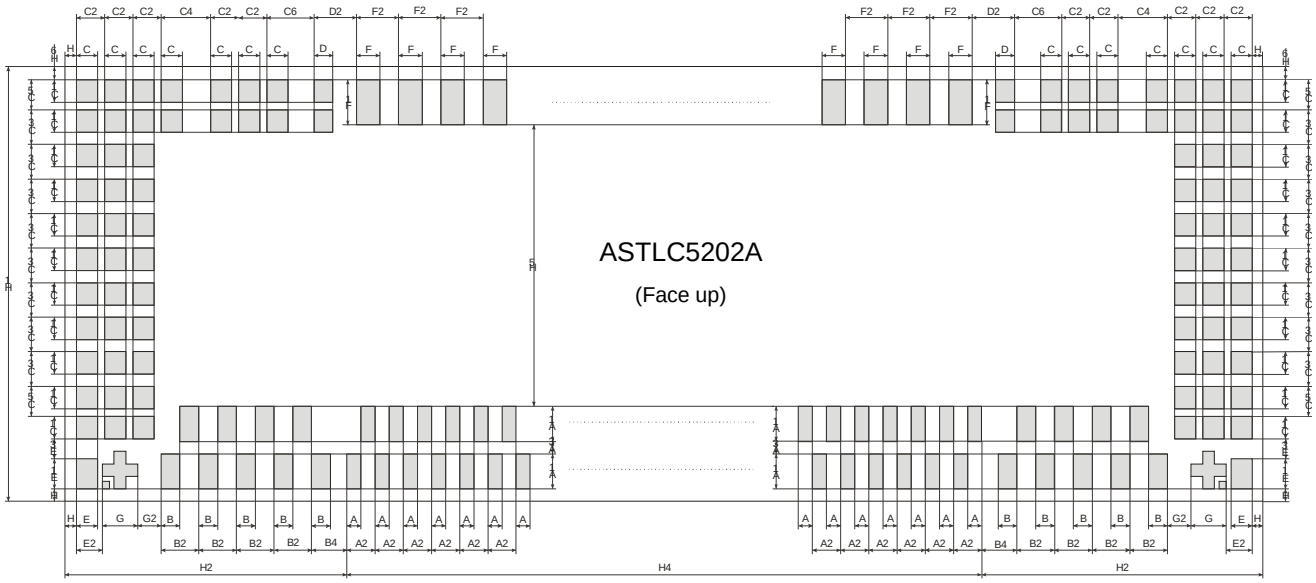

Figure 8: Chip size: 15600μm x 870μm

Note1: Chip size includes scribe line.
Note2: To ensure that the IC functions properly, bond VDD, AVDD, VSS and AVSS pins.
Note3: The 0.1μF capacitor between VDD and VSS and between AVDD and AVSS should be placed to IC as close as possible

Symbol	Size [μm]	Symbol	Size [μm]	Symbol	Size [μm]	Symbol	Size [μm]	Symbol	Size [μm]
A	30	B4	75	C5	60	E2	55	G2	50
A1	70	C	45	C6	100	E3	40	H	20
A2	60	C1	45	D	40	F	50	H1	870
A3	25	C2	60	D2	90	F1	90	H2	600
B	40	C3	69	E	45	F2	90	H4	14400
B2	80	C4	105	E1	60	G	75	H5	562
								H6	23

Note: Distances are given from the edge of the chip (not from the scribe line).

7. REVISION HISTORY

DATE	REVISION #	DESCRIPTION
January 13, 2004	1.0	Datasheet release

8. DISCLAIMER

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9. CONTACT US

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